Asynchronous Ballistic Reversible Fluxon Logic

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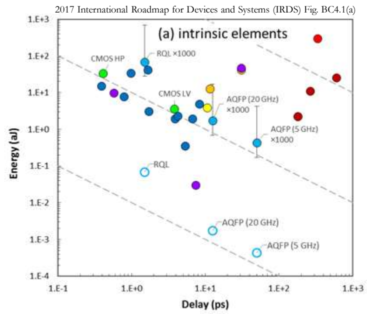
I. Motivation

- Cost-effective high-performance computing (HPC) requires high *computational energy efficiency*, at any given device performance level, in datacenter (room-temperature) settings.
- Existing SCE logic technologies are **not competitive** by such energy-delay metrics after accounting for specific power consumption of cryo-coolers.

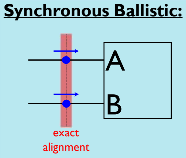


- Improving computational energy efficiency requires approaching the ideal of *reversible computing*, but existing adiabatic approaches for reversible logic in SCE (PQ, nSQUIDs, RQFP) impose substantial clocking-related overheads.
  - High-efficiency clock generation, distribution, and energy recovery is a difficult engineering challenge!
- **Problem Statement:** *Investigate whether/how reversible computing can alternatively be implemented in SCE* ***without*** *externally-driven adiabatic transitions*

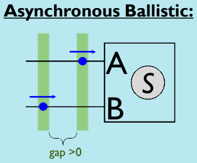
II. Previous work

- Frank '17 introduced *Asynchronous Ballistic Reversible Computing* (ABRC), the first *general* theoretical circuit model of unclocked, universal reversible computation.
  - Data pulses propagate ballistically and asynchronously between devices
    - *And elastically scatter* off devices
  - Local device state updates reversibly on pulse arrival
- **Research Question:** *Can the abstract ABRC model be implemented using ballistically-propagating flux quanta (fluxons) as the signal pulses, and stationary (but mutable) trapped fluxons to register the internal device state?*
  - *While dissipating much less than the fluxon energy per scattering/state-update event?*

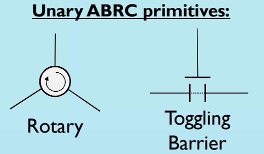
Synchronous Ballistic:



Asynchronous Ballistic:

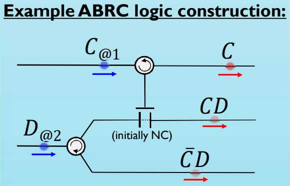


Unary ABRC primitives:



(First set of ABRC primitives proved to be computation universal)

Example ABRC logic construction:



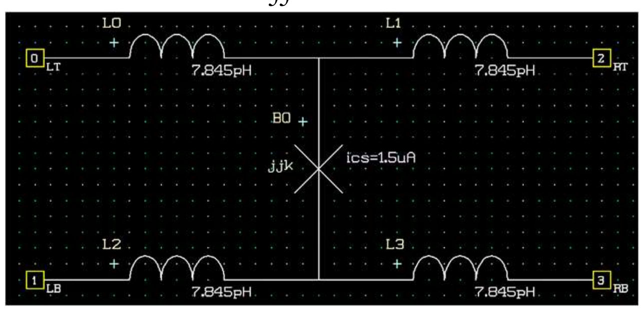
(AND from toggling switch gate)

III. Ballistic interconnects

- Two well-studied methods to propagate fluxons near-ballistically along passive interconnects:
  - Microstrip (or similar) p*assive transmission lines (PTLs)*
    - Support fast pulse propagation velocities
  - *Long Josephson junctions* (LJJs)
    - Support a soliton propagation mode
      - Described by the sine-Gordon equation
    - Can be continuous, or discretized (dLJJ)
- Our initial investigation is focusing on **dLJJ interconnects** for simplicity of modeling
  - Can be implemented in available Nb processes
    - *E.g.*, Hypres S#45/100/200
- Example parameters for dLJJ unit cell:

Parameter description	Sym-bol	Value	Units
Junction critical current density	J_c	1	µA/µm^2
Unit Josephson junction area	A	1.5	µm^2
Unit JJ critical current	I_c	1.5	µA
Round JJ diameter	d	1.38	µm
Intrinsic JJ (shunt) capacitance	C_J	60	fF
JJ intrinsic inductance	$L_J(0)$	220	pH
JJ plasma frequency	ω_J	44	GHz
Drawn cell inductance	L	31.38	pH

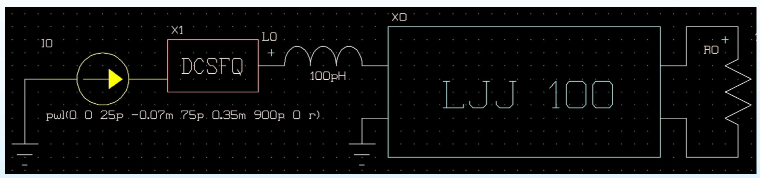
- XIC schematic for dLJJ unit cell:



- JJ model in XIC's `model.lib` file:

```
.model jjk jj(rtype=0, vg=2.8m,
+             icrit=1.5u, cap=60f)
```

- A simple test bench for dLJJ simulation in XIC
  - DC-SFQ converter is from the SUNY RSFQ library



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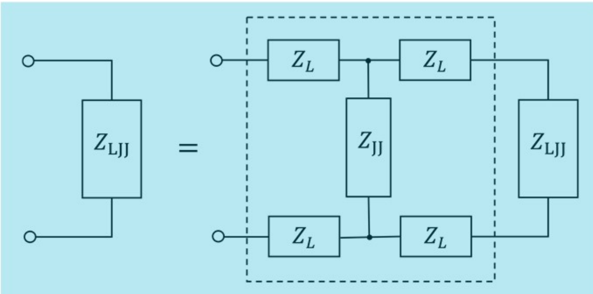
IV. Impedance modeling of dLJJ

- Circuit equivalence for calculating small-signal impedance of a semi-infinite string of dLJJ cells:



- Recurrence relation corresponding to diagram:

$$Z_{\mathrm{LJJ}} = 2Z_L + \cfrac{1}{\cfrac{1}{Z_{\mathrm{JJ}}} + \cfrac{1}{2Z_L + Z_{\mathrm{LJJ}}}} \tag{1}$$

- Solving eq. (1) for line impedance Z_{LJJ} gives us:

$$Z_{\mathrm{LJJ}} = 2\sqrt{Z_L(Z_L + Z_{\mathrm{JJ}})} \tag{2}$$

- Small-signal impedance Z_{JJ} of each JJ is given by:

$$\frac{1}{Z_{\mathrm{JJ}}} = \frac{1}{Z_{\mathrm{J}L}} + \frac{1}{Z_{\mathrm{J}C}} \tag{3}$$

where:

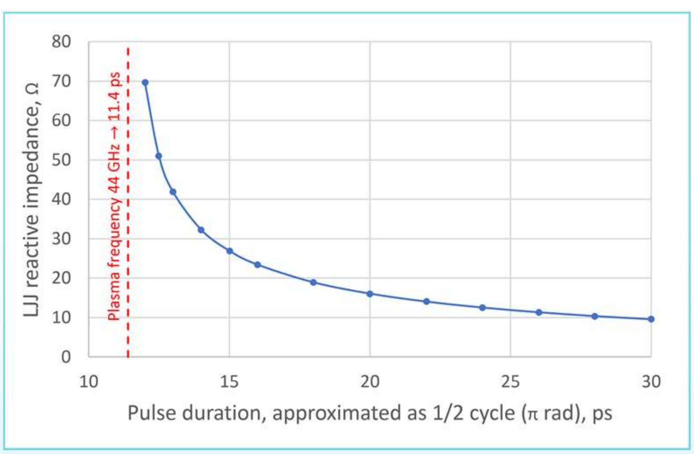
$$Z_{\mathrm{J}L} = j\omega L_{\mathrm{JJ}}(0), \qquad Z_{\mathrm{J}C} = -\frac{j}{\omega C_{\mathrm{JJ}}} \tag{4}$$

and

$$L_{\mathrm{JJ}}(0) = \frac{\Phi_0}{2\pi I_c} \tag{5}$$

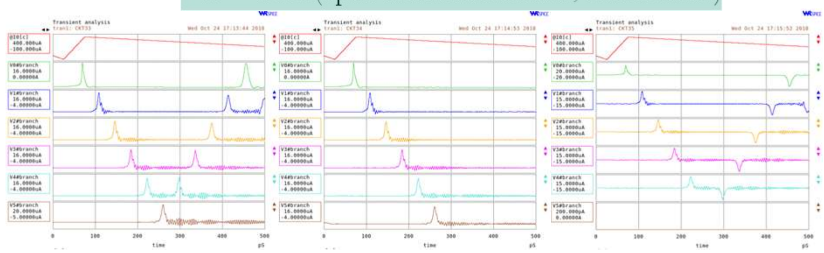
is the JJ intrinsic inductance $L_{\mathrm{JJ}}(\varphi)$ for $\varphi \to 0$.

- Plotting $Z_{\mathrm{LJJ}}(\omega)$ vs. approx. pulse width $\tau = \pi/\omega$:



V. WRSPICE simulations of dLJJ

- For different values of the terminating resistor R:
  1. $R = 0\ \Omega$ (closed-circuit termination; flux conserved)
  2. $R = 16\ \Omega = Z_{\mathrm{LJJ}}$ for $\tau = 20$ ps wide pulses
  3. $R = 1\ \mathrm{G}\Omega$ (open-circuit termination; flux reverses)



- Note we observe a well-defined flux soliton
  - Pulse duration = 20 ps, width = 10.5 dLJJ cells
  - Traverses one dLJJ unit cell every 1.9 ps
  - At 1 pH/µm line inductance, $v \approx c/36$
    - Could probably be increased if desired

VI. Conservation/Symmetry Constraints

- Without considering these, the number of possible ABRC functions with polarized I/O pulses and states would be unmanageable:

No. of I/O Ports	Number of I/O Syndromes	Number of Fully Reversible Functions
1	6	6! = 720
2	12	12! = 479,001,600
3	18	18! = 6,402,373,705,728,000
4	24	24! = 620,448,401,733,239,439,360,000

- But: A planar circuit with a closed superconducting boundary conserves net flux threading the boundary
  - Due to Meissner-effect flux trapping
- And: Any circuit with only inductors, capacitors, and JJs is *time-reversal symmetric*
  - Dynamics is identical if all currents & fields reversed
- Such constraints limit the number of implementable 1-3 port ABRC functions to a relatively small subset, which will be detailed in future work
  - **Example:** The only non-trivial 1-port operation is *Swap*, which exchanges external & internal fluxons, and acts as a reversible memory.

Input Syndrome		Output Syndrome
+1(+1)	→	(+1)+1
+1(−1)	→	(+1) −1
−1(+1)	→	(−1)+1
−1(−1)	→	(−1)−1

VII. Conclusion

- Preparatory work on this project is complete, and we are now ready to begin detailed design work to find JJ circuits that implement useful ABRC functions.

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